

# High Performance of Liquid-Gated Silicon Nanowire FETs Covered with Ultrathin Layers of Diamond-Like Tetrahedral Amorphous Carbon

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Label-free, low-noise, and ultrahigh-sensitive biosensors based on liquid-gated silicon (Si) nanowire (NW) field-effect transistors (FETs) have recently emerged as promising diagnostic tools that can be used for healthcare monitoring and point-of-care applications. However, the sensing capabilities and performance of such devices still critically depend on several factors, including the quality and intrinsic properties of the materials used. In particular, the important role of determining device performance is assigned to the gate insulator layer, which acts as a sensing surface in such NW-based biosensors and still requires optimization. Herein, several advanced multilayer structures: Si NW/SiO<sub>2</sub>/diamond-like carbon FETs, are investigated. The high quality of the diamond-like carbon layer obtained by low-temperature physical vapor deposition is confirmed by X-ray photoelectron spectroscopy and Raman spectroscopy studies. Current-voltage and noise spectroscopy reflect the high-quality transport properties in these structures.

## 1. Introduction

Silicon nanowire (NW) field-effect transistor (FET) structures demonstrate unique properties for the label-free, high-speed detection of different biomarkers.<sup>[1–5]</sup> The structures can be fabricated using complementary metal-oxide-semiconductor (CMOS)-compatible technology. They are therefore promising for mass production, which is very important for biosensing applications with respect to personalized medical detection

platforms. Despite tremendous progress in this field of research, a number of challenges still need to be overcome to ensure that such unique devices can be made available on the market. One of the main challenges is the issue of reliability, that is, reproducible device operation in a liquid environment.


At present, native or thermally grown SiO<sub>2</sub> oxide does not satisfy stability criteria. However, silicon dioxide obtained on bare silicon surface using thermal oxidation should be used, as it enables the lowest defect density at the Si/SiO<sub>2</sub> interface.<sup>[6]</sup> In addition, new materials covering the SiO<sub>2</sub> layer may therefore result in the improved stability of NW FET operation through contact in bioliquid. They should be studied, followed by several steps

of device optimization to obtain a reliable signal-to-noise ratio. One promising material is diamond, as this wide bandgap material is expected to be stable in a liquid environment. There have already been several reports on FETs working on the basis of a single diamond channel. With its remarkable electrothermal properties, such as the highest known thermal conductivity ( $\approx 22 \text{ W cm}^{-1} \text{ K}^{-1}$  at RT), high critical electric field ( $> 10 \text{ MV cm}^{-1}$ ), and large bandgap (5.47 eV), diamond may provide advantages for power FET devices.<sup>[7]</sup> Diamond as a single thick material channel of an FET demonstrates promising properties for biosensors. It possesses high chemical stability and biocompatibility.<sup>[8]</sup> However, obtaining such a relatively thick layer is not compatible with CMOS technology and it is an expensive material.

The temperature at which deposition is performed is the crucial parameter. Research into the optimization of chemical vapor deposition (CVD) diamond coatings began in the 1980s. The optimum substrate temperature was found to be about 800 °C during the growth of diamond through a series of test runs. A temperature range from 500 to 1200 °C is currently used in CVD methods to grow high-quality diamonds.<sup>[9]</sup> This is a significant drawback, as such temperatures are not compatible with CMOS technology. Low-temperature growth should be used for fine silicon nanowire FET applications to utilize the full potential of CMOS-compatible biosensors. Therefore, attempts are currently being made to find novel approaches for the fabrication of multilayer structures utilizing CMOS-compatible fabrication technology. According to theoretical predictions,

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the mobility of nanowire can be increased in the case of nanowire covered with a diamond layer<sup>[10]</sup> by removing the heating effect, as previously studied in ref. [11]. However, if deposited directly on silicon nanowire, carbon introduces scattering centers, which results in the deterioration of FET transport properties. Therefore, the optimum dielectric stack should be determined to retain a high level of mobility and to improve stability in the liquid of NW FET structures.

The issue of drift in FET structures was studied in refs. [12,13] for several dielectric layers, with the exception of diamond-like material. Being directly exposed to the electrolyte solution, the surface of NWs is affected by the ionic solution, which leads to the irreversible degradation of the material properties and, in turn, the deterioration of the operating parameters of underlying FETs. Therefore, the development of reliable Si NW FET biosensors requires experimental conditions to be optimized and the material quality further improved to enable the hysteresis- and leakage-free operation of such NW FET-based devices in a liquid media. When considering diamond-like carbon (DLC) as a possible candidate for the top layer, a distinction must be made between hydrogen-containing (a-C:H) and hydrogen-free (a-C or ta-C) films. Due to the electrically insulating property, a-C:H coatings are rather not suitable, whereas the hydrogen-free DLC coatings can be considered. In particular, ta-C coatings, which can reach an  $sp^3$  content of up to 85% and are thus very similar to diamond in terms of bonding character, could therefore be an alternative to diamond for NW FET application. ta-C coatings are already used industrially in some applications due to their outstanding mechanical and tribological properties.<sup>[14,15]</sup> Compared to a-C:H, ta-C-coatings show higher thermal stability and relatively large bandgap,<sup>[16]</sup> depending on the  $sp^3$ -content. A special feature is that ta-C forms a dense and resistant protective layer even as an ultrathin film. It has therefore been used, for example, as a protective top coat for magnetic hard disk drives and read heads.<sup>[17]</sup> There were also microstructural studies on ultrathin ta-C films in the thickness range of 1–10 nm, which showed that homogeneous and ultrasmooth films with predominant  $sp^3$  bonding are formed above 1–2 nm film thickness.<sup>[18]</sup> To summarize, thin ta-C films should have a very promising potential to be used as a novel coating gate dielectric material for such liquid-gated (LG) NW FET devices. To the best of the authors' knowledge, ta-C has not yet been considered for this application.

In this work, we fabricated and investigated the electrical performance of LG Si NW FETs covered with a new gate dielectric stack consisting of an 8 nm thin thermally grown  $SiO_2$  layer and a diamond-like film: a 5 nm thin tetrahedral amorphous carbon (ta-C) film. No heating was applied for the deposition of the ta-C to avoid any thermal effect to the gate dielectric stack. Such NW FET structures operating in a liquid environment demonstrate advanced properties. Our results show in particular an improved stability and pH sensitivity of the biosensor structures.

## 2. Results and Discussion

### 2.1. Diamond-Like Material Characterization

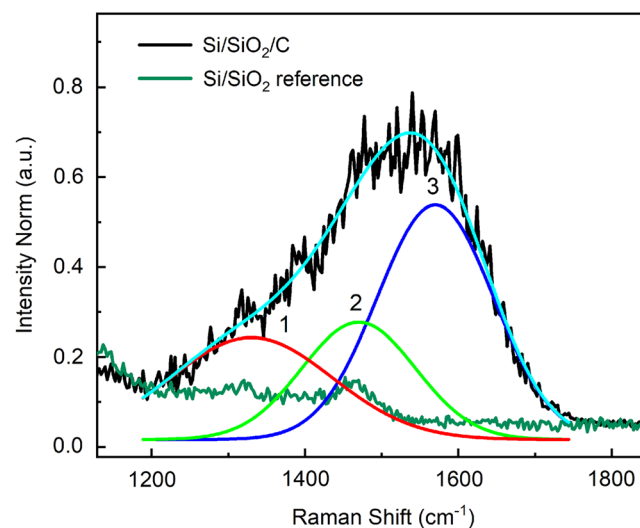
A nominal coating thickness of 5 nm was chosen for the ta-C coatings because this was assumed to be the minimum thickness

for a closed, uniform, dense, and smooth diamond-like carbon layer with a high  $sp^3$  content. The coating thickness of 5 nm was set using the scaled coating time of a previous reference test with coating thickness determined by laser interferometry. An additional Si sample codeposited with the Si NW FETs was subsequently measured in thickness by X-ray reflectometry (XRR). The measured film thickness was about 6 nm, which is in good agreement with the nominal film thickness.

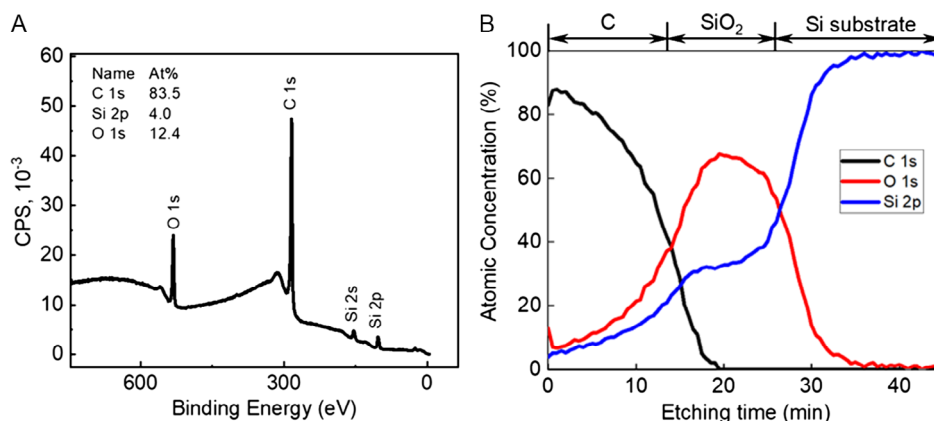
Raman and XPS measurements were performed to study the structure and bonding state of ta-C films on the  $SiO_2$ -covered samples. The corresponding results are shown in Figure 1 and 2, respectively.

The Raman measurements demonstrate a relatively broad peak for the Si/ $SiO_2$ /C structure. The spectrum was analyzed by decomposition to three peaks: 1 (red) –  $1330 \pm 61 \text{ cm}^{-1}$ , 2 (lime) –  $1471 \pm 4 \text{ cm}^{-1}$ , and 3 (blue) –  $1572 \pm 3 \text{ cm}^{-1}$ , respectively. It should be noted that crystalline diamond films are nearly fully  $sp^3$ -bonded carbon, demonstrating a sharp Raman peak at  $1332 \text{ cm}^{-1}$  wave numbers. In contrast, amorphous, diamond-like carbon structures like ta-C and a-C:H display a broad G-peak with a maximum around  $1570 \text{ cm}^{-1}$  and, depending on the  $sp^2$ -content a more or less pronounced D-peak with a maximum around  $1555 \text{ cm}^{-1}$ . The existence of a D-peak is evidence of ordered atomic structures of  $sp^2$ -atoms in graphenic rings.<sup>[19]</sup> The extracted blue curve for the ta-C coating in Figure 1 shows a pure G-peak at a typical position of highly  $sp^3$ -bonded amorphous carbon and there is no evidence of D-peak, that is, clustered  $sp^2$ -regions. Therefore, it can be concluded that despite the small film thickness of only 5 nm, a high  $sp^3$ -containing ta-C layer is present on the surface  $SiO_2$ -covered samples.

The results are consistent with the data obtained from X-ray photoelectronspectroscopy (XPS) (Phi5000 VersaProbeII,



**Figure 1.** Raman spectra measured for Si/8nm $SiO_2$  (green) and Si/8nm $SiO_2$ /5 nm ta-C (black) structures. The black curve after averaging (cyan curve corresponding to the Si/ $SiO_2$ /ta-C structure) can be decomposed using a three-peak approximation. The three peak positions were identified as follows: 1 (red) –  $1330 \pm 61 \text{ cm}^{-1}$ , 2 (lime) –  $1471 \pm 4 \text{ cm}^{-1}$ , 3 (blue) –  $1572 \pm 3 \text{ cm}^{-1}$ .

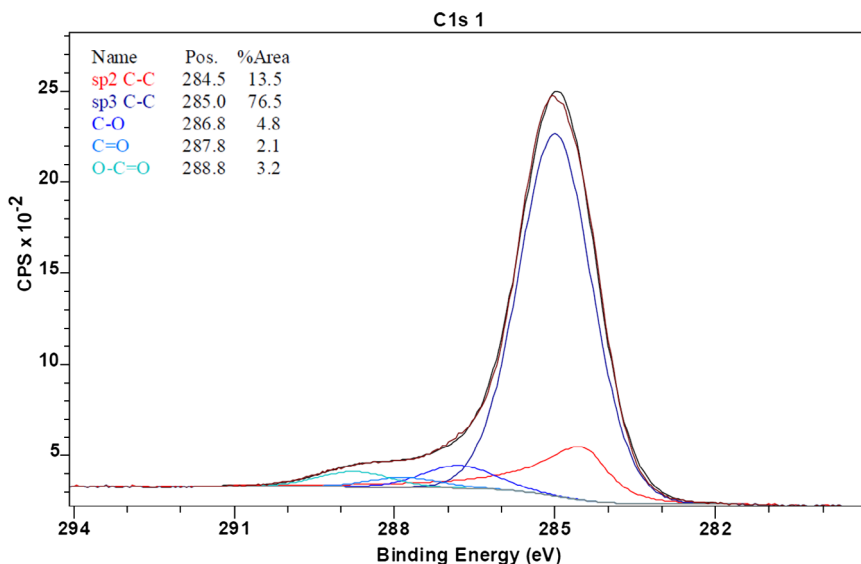


**Figure 2.** a) XPS spectrum measured for Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures (inset shows a quantification table of the atomic percentages of elements with an error of 10%, normalized to 100 at%, Shirley background). b) XPS depth profiles obtained using Ar ion etching for Si/8 nm SiO<sub>2</sub>/5 nm ta-C, showing the structure composition of C (black curve), O (red curve), and Si (blue curve) as an atomic percentage. The inset at the top shows the schematic of the device layer structure.

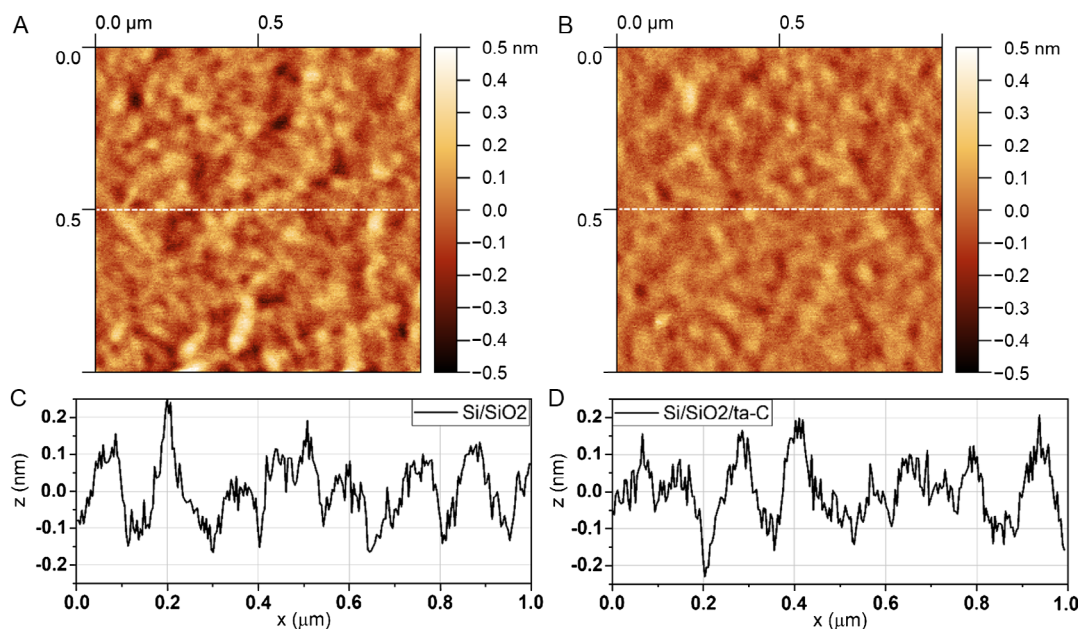
ULVAC-Phi Inc., USA Source: Al K-alpha, monochromatic (1.486 keV)). The data confirm that the uniform hydrogen-free ta-C layer was successfully deposited on top of the SiO<sub>2</sub>-covered Si structures. The XPS spectrum measured for the Si/SiO<sub>2</sub>/ta-C structure is shown in Figure 2a. There is a strong peak corresponding to C, which reflects the high quality of the deposited carbon layer. The depth profiles were also measured for this sample using Ar<sup>+</sup> ions etching at 0.5 kV energy. Analysis of XPS spectra over etching time provides the depth profiles (Figure 2b). The depth profiles of the sample reflect that the 5 nm thin carbon layer is very well separated from silicon by a thin (8 nm) SiO<sub>2</sub> material. The interfaces between carbon and SiO<sub>2</sub> as well as between SiO<sub>2</sub> and Si can be clearly identified. This shows that carbon does not penetrate into the Si material and does not introduce the scattering into this layer.

Figure 3 shows XPS spectra in the region from 294 to 281 eV. XPS spectra can be deconvoluted into five component peaks with binding energies, *E* (eV), at about 284.5:285.0:286.8:287.8:288.8 eV. The peak at 286.8 eV corresponds to the vibrations of C–O bonds and peak at 288.8 eV corresponds to stretching vibrations of O=C=O in carboxyl groups. Additional small contributions have been found from measured XPS data: carbonyl groups: C=O. The peak at 284.5 eV and the peak at 285.0 correspond to the carbon allotropes with *sp*<sup>2</sup> (13.5%) and *sp*<sup>3</sup> (76.5%) hybridized bonds, respectively.

Moreover, the carbon layer shows perfect uniformity. The results of the surface smoothness study for Si/8 nm SiO<sub>2</sub> and Si/8 nm SiO<sub>2</sub>/5 nm ta-C are shown in Figure 4a,b, respectively. The data in Figure 4b reflect the improved morphology of Si/8 nm SiO<sub>2</sub>/5 nm ta-C compared to Si/8 nm SiO<sub>2</sub>. The improved



**Figure 3.** XPS spectrum measured for Si/8 nm SiO<sub>2</sub>/5 nm C structures (inset shows a quantification table of the atomic percentages of elements with an error of 10%, normalized to 100 at%, Shirley background). The diamond-like structure represents the carbon allotropes with *sp*<sup>2</sup> (13.5%) and *sp*<sup>3</sup> (76.5%) hybridized bonds.

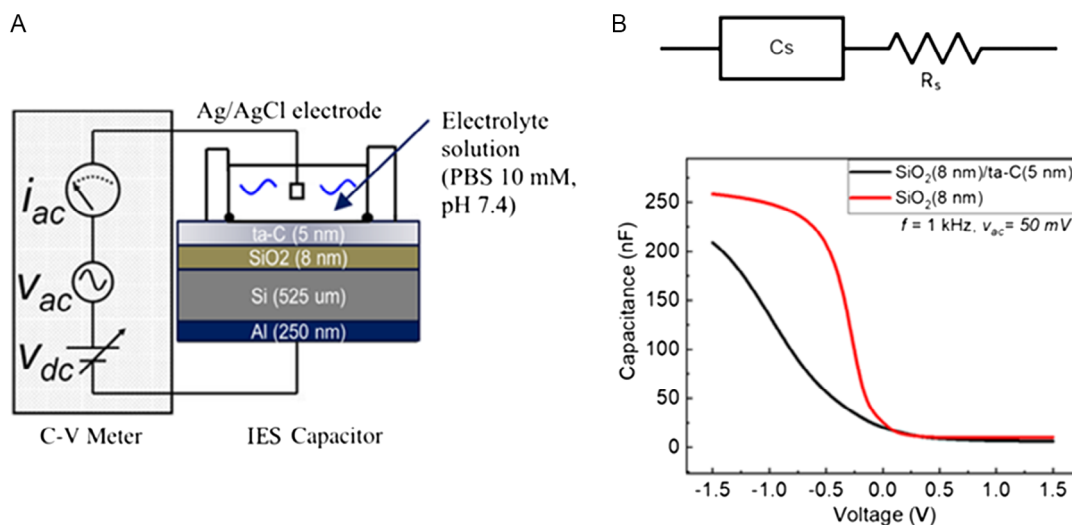


**Figure 4.** AFM characterization of the reference Si/SiO<sub>2</sub> sample a,c), and the ta-C-coated Si/SiO<sub>2</sub>/ta-C sample b,d). The root mean square height for the characterized area of 1 μm<sup>2</sup> is calculated as RMS = 0.104 nm for the SiO<sub>2</sub> surface and RMS = 0.077 nm for the ta-C surface. Profile lines (c) and (d) were acquired from the topographic images (a,b), respectively, (positions are defined by dashed white lines).

morphology of Si/8 nm SiO<sub>2</sub>/5 nm ta-C compared to Si/8 nm SiO<sub>2</sub> can be explained by the formation of a smooth, dense, and uniform amorphous ta-C coating. A smoothing effect on the atomic roughness scale is possible because ta-C coating is a high-energy ion subplantation coating process. The high level of smoothness is surprising after the deposition. Despite a thin layer of carbon, the level of roughness even decreased after its deposition onto the SiO<sub>2</sub> dielectric. Quantitatively, this improvement can be presented as the root mean square value of ordinate values within the defined area. It is equivalent to the standard deviation of heights.

## 2.2. Electrical Properties of Carbon-Covered Structures

To study the electrical characteristics of Si/8 nm SiO<sub>2</sub> and Si/8 nm SiO<sub>2</sub>/5 nm C structures, two different experiments were performed: capacitance–voltage characterization of flat electrolyte insulator semiconductor (EIS) structures in liquid and current–voltage characteristics of nanowire FET structures. Measured C–V characteristics of flat planar samples are shown in **Figure 5**. The technique is widely used to determine semiconductor parameters and obtain values relating to oxide thickness, oxide charge, ion mobility, and the density of interface traps. It



**Figure 5.** a) Schematic representation of the measurement system for thin-film dielectric layer studies in aqueous solutions. b) Measured C–V characteristics for Si/8 nm SiO<sub>2</sub> and Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures.

yields quantitative information about diffusion layer thickness and doping concentration in semiconductor materials as well as layer structure parameters. A pseudo-reference electrode was immersed in the phosphate-buffered saline (PBS) solution (electrolyte) and PBS was in direct contact with the ta-C layer. The measurement cell connected to the impedance analyzer was biased by a direct-current (DC) voltage source. Impedance measurements were conducted at an alternating-current (AC) voltage signal of 1 kHz and an amplitude of 50 mV. The contact between the electrolyte and the measured structure is limited by a rubber O-ring and was equal to  $0.44 \text{ cm}^2$ . A voltage sweep was performed in a range  $(-1.5; 1.5) \text{ V}$  with a sweeping rate of  $10 \text{ mV s}^{-1}$ .

Capacitance measured using the impedance meter is dependent on the applied DC voltage. The  $C$ - $V$  characteristic measured for the Si/SiO<sub>2</sub>/electrolyte system has a typical shape for the high-frequency measurement using the MOS capacitor with distinct accumulation, depletion, and inversion regions. The  $C$ - $V$  characteristic obtained for the Si/8 nm SiO<sub>2</sub>/5 nm ta-C structure differs significantly compared with the Si/SiO<sub>2</sub> structure. The changes are obvious in comparison with the reference samples covered only by a SiO<sub>2</sub> layer (Figure 5b), demonstrating that the thin carbon layer is stable after contact with the PBS liquid.

Measuring the  $C$ - $V$  curves repeatedly over time allows us to observe a flat-band voltage behavior as a function of time

(Figure 6). From the linear region, we obtain the flat-band voltage, which we use as a tracking parameter for biosensing.

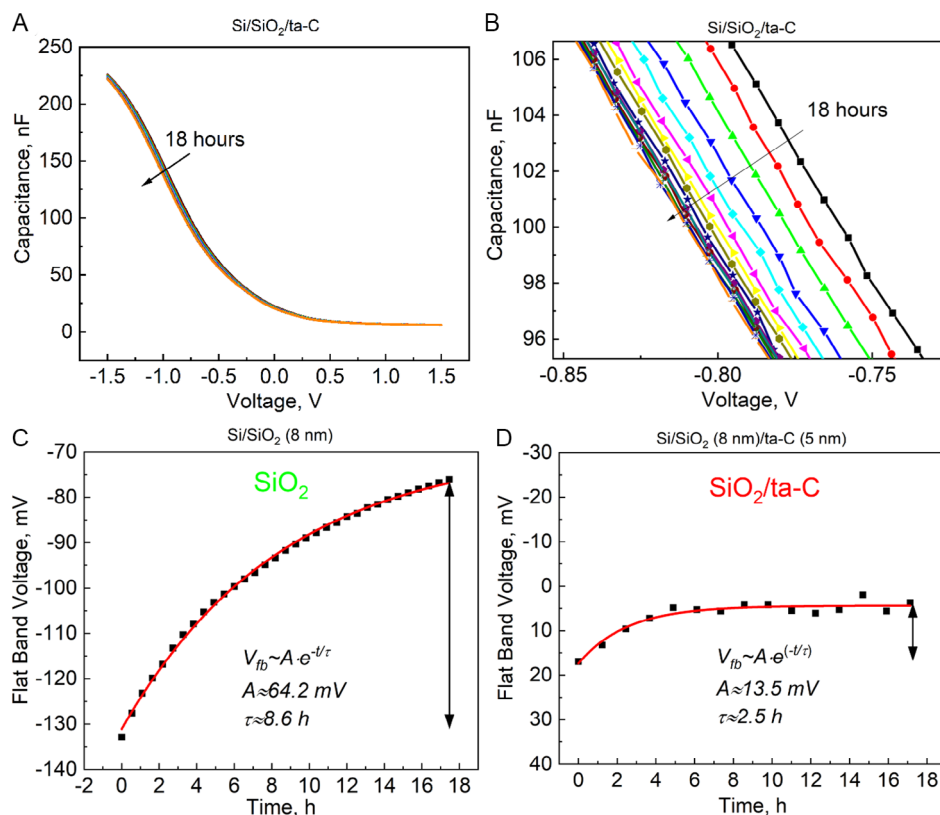
To analyze the data, we use a Mott-Schottky plot when we have  $1/C^2$  over voltage dependence according to Equation (1)

$$\frac{1}{C^2} = \frac{1}{C_{\text{ox}}^2} + \frac{2(V - V_{\text{fb}})}{\epsilon \epsilon_0 A^2 e N_{\text{D}}} \quad (1)$$

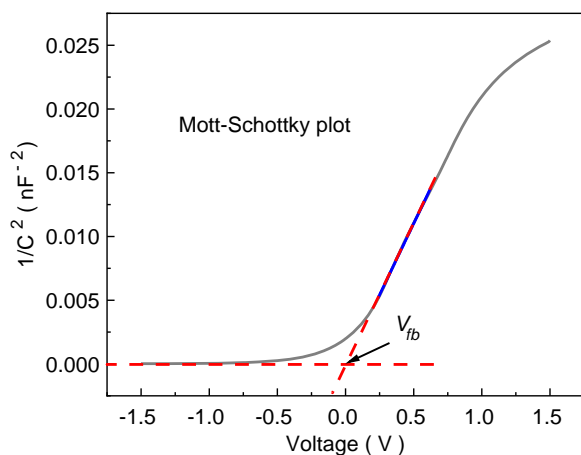
where  $C$  is the capacitance of the EIS structure,  $C_{\text{ox}}$  is the capacitance of only oxide (SiO<sub>2</sub>) or dielectric layer (SiO<sub>2</sub>/ta-C),  $\epsilon_0$  is the vacuum permittivity,  $\epsilon$  is the relative permittivity of semiconductor (Si),  $A$  is the EIS capacitor area (area of the contact between electrolyte and SiO<sub>2</sub>/ta-C layer),  $e$  is the elementary charge,  $N_{\text{D}}$  is the doping density of Si substrate,  $V_{\text{fb}}$  is the flat-band voltage.

Typical Mott-Schottky plot obtained for SiO<sub>2</sub> covered by ta-C is shown in Figure 7.

For comparison, a flat-band voltage drift is measured (Figure 6c) under the same conditions for the Si/SiO<sub>2</sub> structure, for which the drift is in a range of 60 mV. The obtained time dependence of the flat-band voltage studied for Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures shows relatively small drift (13.5 mV) Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures. It should be emphasized that the shape of the  $C$ - $V$  characteristic measured for the structure covered by a diamond-like layer does not change after 4 h of



**Figure 6.** Time-dependent investigation of the  $C$ - $V$  characteristics shift measured for a) Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures in PBS solution. Each curve was measured under the same conditions for a period of 1 h; b) Enlarged  $C$ - $V$  characteristics of a) shift measured for Si/8 nm SiO<sub>2</sub>/5 nm ta-C. c) The flat-band voltage obtained from the  $C$ - $V$  characteristics for Si/8 nm SiO<sub>2</sub> and d) The flat-band voltage obtained from the  $C$ - $V$  characteristics for Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures as a function of time. The data represent the difference in drift for two types of samples and improved stabilization for Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures compared to Si/8 nm SiO<sub>2</sub> structures.



**Figure 7.** Mott-Schottky plot was obtained according to Equation (1) for each of measured  $C-V$  characteristics to find flat-band voltage precisely.

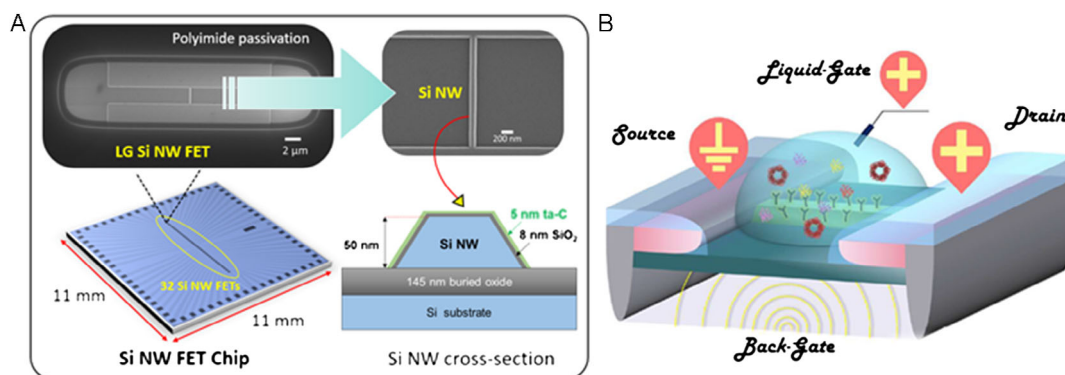
stabilization in a PBS liquid. The amplitude of the drift voltage is four times smaller compared to the amplitude obtained for the Si/8 nm  $\text{SiO}_2$  structures. In the case of the latter structures with

only an 8 nm  $\text{SiO}_2$  layer, the stable state was still not reached after 18 h. The main reason for the difference is the dense and smooth ta-C layer preventing penetration of ions from liquid due to strong C bonds of forming  $sp^3$  compositional diamond-like material.

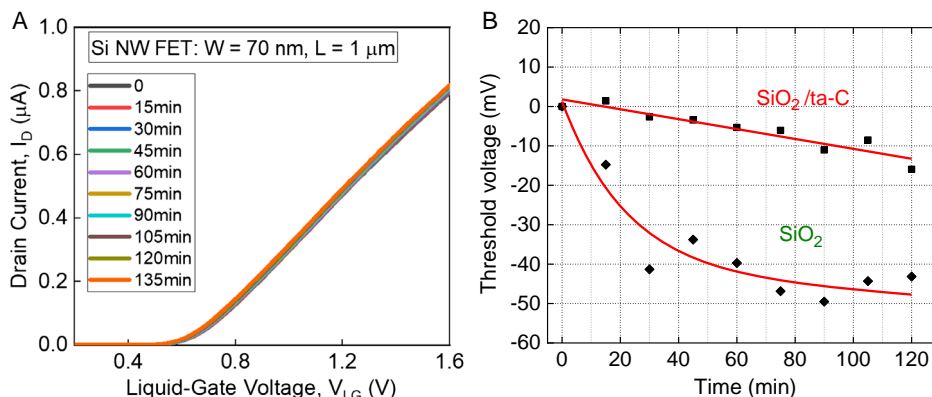
Characterization of the electrical properties of fabricated nano-wire FET structures was studied using current-voltage curves. The schematic illustration and composition of a typical fabricated Si NW chip containing 32 independent single Si NW FETs are shown in **Figure 8**.

A set of NW FET devices covered with  $\text{SiO}_2$  and  $\text{SiO}_2/\text{ta-C}$  layers was measured in a PBS solution as a function of time to study device stability and reproducibility. **Figure 9a** shows the  $I-V$  characteristics measured with a time step of 15 min for NW FET devices covered  $\text{SiO}_2/\text{ta-C}$  layers.

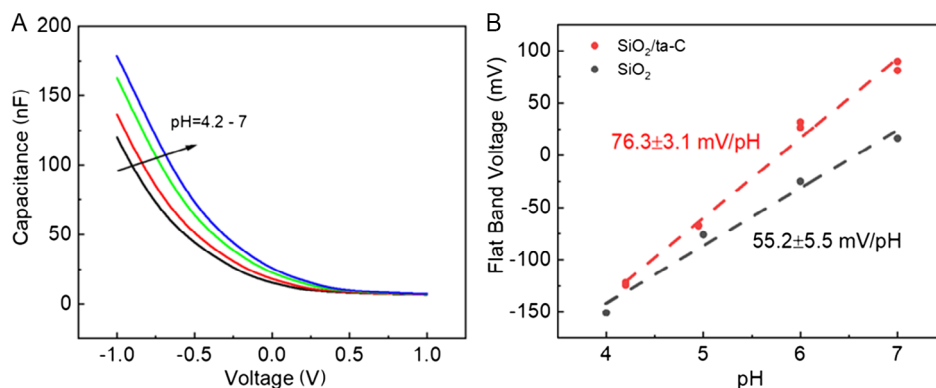
As can be seen, the  $I-V$  characteristics of the device demonstrated good working stability and repeatability even after being exposed to the ionic solution for a relatively long period of time. It should be noted that the leakage current through the front-gate dielectric layer remained negligibly small (below 10 pA) when measured in the LG configuration, confirming the good stability properties of the fabricated sensors.  $I-V$  transfer curves



**Figure 8.** a) Schematic illustration and composition of a typical fabricated Si NW  $11 \times 11 \text{ mm}^2$  chip with 32 Si NW FETs. SEM images of the transistor itself and a single Si NW as a transducer. Schematic cross section of the Si NW after ta-C deposition. Liquid-gated measurement for Si NW FET; b) the configuration of the measurements is shown in the right-hand image. A liquid gate was used for gating a structure.



**Figure 9.** a) Set of transfer curves measured for a 70 nm wide and  $1 \mu\text{m}$  long ta-C-covered Si NW FET immersed in PBS solution with a pH of 7.4 and an ionic strength of 10 mM, b) threshold voltage change in time measured for the NW FET covered with  $\text{SiO}_2/5 \text{ nm ta-C}$  compared with the NW FET covered with  $\text{SiO}_2$ . The data are normalized by subtraction of value of starting threshold voltage.



**Figure 10.** a) C–V characteristics of the Si/SiO<sub>2</sub>/ta-C structure measured in different pH buffer solutions and b) flat band voltage change as a function of pH demonstrating improved pH sensitivity of Si/8 nm SiO<sub>2</sub>/5 nm ta-C structures compared to Si/8 nm SiO<sub>2</sub> ones.

measured for the Si NW/8 nm SiO<sub>2</sub>/5 nm ta-C structure in liquid demonstrate good reproducibility. Good stability of the NW FET covered with SiO<sub>2</sub>/5 nm ta-C compared with the NW FET covered with SiO<sub>2</sub> was also achieved (Figure 9b). The data are normalized by subtraction of value of starting threshold voltage. The behavior of the NW FET device structures correlates with the properties obtained for EIS flat structures using C–V characteristics (Figure 10).

Buffers were exchanged every 10 min. The extracted values of the flat-band voltages are plotted against the pH value of the solutions. For comparison, the same measurement was carried out for the Si/SiO<sub>2</sub> reference sample. The results show that the flat-band voltage shift to a positive direction with increasing pH value, which is in good agreement with the changes in proton concentration.

It should be noted that structures covered with carbon demonstrate higher sensitivity compared to Si/SiO<sub>2</sub> reference samples. The supra Nernstian pH sensitivity, higher than 59 mV pH<sup>−1</sup>, the Nernst limit, is in agreement with values sensitivity reported for the case of bulk diamond channel,<sup>[20]</sup> where suprasensitivity is explained as one of hypothesis by the percolation behavior of the interconnected conductive regions formed between source and drain contacts.

### 3. Conclusion

In this study, LG Si NW FETs for ultrahigh-sensitive biosensor application were covered with a 5 nm thin tetrahedral amorphous carbon (ta-C) film on a gate dielectric stack consisting of an 8 nm thin thermally grown SiO<sub>2</sub> layer. By Raman and XPS spectroscopy, it could be shown that despite the thickness of only about 5 nm, a closed ta-C type carbon film with a predominant sp<sup>3</sup> content is present. We showed that Si NW FETs covered with a ta-C/SiO<sub>2</sub> gate dielectric stack deposited close to room temperature demonstrate good electrical properties and acceptable stability while operating in liquids, even for a long time. The designed devices are promising for biosensing applications with good stability and reliability in biological liquids and body fluids in comparison to devices not covered by a diamond-like film. Advanced pH sensitivity was demonstrated at the level of 76 mV pH<sup>−1</sup>.

### 4. Experimental Section

A nominally 5 nm thick ta-C coating was deposited on the flat samples (Si/SiO<sub>2</sub>) and on the Si NW FET using plasma-filtered pulsed laser-arc technique<sup>[21]</sup> within a commercial physical vapor deposition (PVD) coating system (DREVA 600, VTD Vakuumtechnik Dresden, Germany). For deposition, the specimens were mounted in single-rotation arrangement. Prior to carbon coating, Ar<sup>+</sup>-ion etching was performed using a linear anode-layer source. The deposition time was 70 s using a pulsed-arc current of 1600 A in maximum at a pulse frequency of 75 Hz. No external heating, no oxygen gas, and no bias voltage were applied during deposition.

The ta-C coating thickness was adjusted via the length of the coating time after a previous reference test with a larger coating thickness by calculating the coating thickness ratio. The thickness measurement of the reference test was carried out with the laser interference method. In parallel to the original samples, a flat piece of silicon was coated and the ta-C layer thickness was subsequently determined by means of XRR. A D5005 reflectometer from Bruker AXS with a Cu-Kα parallel beam arrangement (double Göbel mirrors) was used for this purpose. A knife-edge with a distance of approx. 25 μm to the sample surface was used to limit the measuring spot in beam direction (x). In y-direction, the footprint of the beam was defined by an aperture of about 2 mm.

For the fabrication of capacitive carbon-covered electrolyte insulator semiconductor (EIS) structures, we used a high-quality, single-side-polished p-type silicon wafer (B concentration of approximately 2 × 10<sup>15</sup> cm<sup>−3</sup>) with (100) orientation as a substrate (manufactured by Siebert Wafer). First, the wafer was cleaned with piranha solution following a standard RCA procedure, which involved the removal of organic contaminants, oxide stripping, and the removal of ionic contamination. An 8 nm silicon oxide layer was then thermally grown. The front (polished) side of the wafer was protected by a photoresist (AZ 5214E), and the back-side oxide of the wafer was removed in a buffered oxide etchant (BOE 7:1). Aluminum was then deposited onto this side. A protective photoresist was removed during cascade cleaning in acetone and isopropanol. Annealing was subsequently performed at 450 °C for 10 min to provide ohmic contact between the deposited aluminum and the Si substrate. After the fabrication process, the wafers were cut into 1 cm × 1 cm pieces. These fabrication steps were performed at Forschungszentrum Jülich's Helmholtz Nano Facility (HNF). Several samples were additionally subjected to tetrahedral amorphous carbon (ta-C) coating.

Si NW FETs were fabricated according to a previously reported protocol.<sup>[3]</sup> The surface of the chip was covered with a 1.5 μm thick polyimide passivation layer to protect the device against liquid media during electrical measurements. Openings in the passivation layer that only provided liquid solution with access to NW regions were defined by photolithographic patterning. Initially, Si NWs were covered with the 8 nm thin SiO<sub>2</sub> layer that was thermally grown at 850 °C for 45 min during

the fabrication process. To ensure better performance and working stability while operating in a liquid, the nanostructures were additionally covered with the 5 nm thin ta-C film in the same PVD process, as described above.

To perform the confocal Raman microscopy, the samples were illuminated with 532 nm radiation excited with a single-mode frequency doubled Nd:YAG laser via a 100 lm single-mode glass fiber. The measurements were performed at room temperature in backscattering geometry using a Witec 300 alpha R setup with a spectral resolution about  $2\text{ cm}^{-1}$ . We used a Zeiss LD EC Epiplan-Neofluar x50/0.55 objective and the laser power at the back of the objective was 12 mW. An edge filter was utilized to separate the Raman signal from the excitation line. Confocality of the Raman signal was achieved via a 50  $\mu\text{m}$  multimode fiber glass between microscope and the Raman spectrometer, where the fiber serves as a pinhole. The Raman spectrometer was equipped with a holographic grating of 600 lines  $\text{mm}^{-1}$ . As detector a Newton Andor EMCCD camera with  $1600 \times 200$  pixels was used.

To measure the roughness of the samples a Bruker Dimension Edge AFM system is used in tapping mode in air conditions. The scan parameters are the following: scan size ( $1 \times 1\text{ }\mu\text{m}$ ), scan rate ( $1\text{ }\mu\text{m s}^{-1}$ ), and resolution (samples/line of 256). NanoDrive v8.06 software and NanoScope Analysis 2.0 software are applied for imaging and topological analysis. A new tip TESP (<https://www.brukerafmprobes.com/p-3843-tesp-v2.aspx>) is used. Parameters for the image corrections: the fitting and the filtering for AFM image are the following: correction of horizontal scars (strokes) and aligning rows by polynomial method (degree 5).

X-ray photoelectron spectroscopy (XPS) studies were performed using Phi5000 VersaProbe II, ULVAC-Phi Inc., USA, equipped with Al K-alpha, monochromatic (1.486 keV) source. X-ray setting used for the measurements are following: 50 W, 15 kV, 200  $\mu\text{m}$  spot. Charge correction is performed by setting the main component of the C 1s peak to 285 eV for the surface measurement and the Si 2p<sub>3/2</sub> to 99.16 eV for the etched samples.

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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

diamond-like carbon, liquid-gated transistors, low-temperature physical vapor deposition, nanowire field-effect transistors, transport properties

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